Both the amended and the originally filed Figures 10-12 clearly illustrate circuitry 40 with a line width approximately less than the diameter of the plated through hole12, and the examiner's objection on this point is not believed to be well taken.

Upon indication of acceptability, formal drawings will be prepared incorporating the changes indicated.

Claim Rejections – 35 USC § 112:

Claims 12 and 18-20 are rejected under 35 USC § 112, second paragraph, as being indefinite.

Claim 9 has been amended to provide that the at least one filled plated through hole has an outside diameter, and that the circuitry has circuit lines having a line width. Claim 12 has been amended to state that the *circuitry* further comprises pads, not the circuit lines. Amended claims 9 and 12 are now believed to be definite under 35 USC § 112, second paragraph.

Claims 18-20 have been amended to state that the circuitry is disposed on a top surface of the layer of dielectric material. Claims 18-20 are now believed to be definite under 35 USC § 112, second paragraph.

Claim rejections – 35 USC § 103:

Claims 9-20 are rejected under 35 USC § 103(a) as being unpatentable over Jones et al (U.S. Patent No. 5,097,593) in view of Lan et al (U.S. Patent No. 5,906,042.)

Claim 11. Claim 11 claims a printed wiring board comprising circuitry having an aspect ratio greater than about one. Contrary to the examiner's assertion, Jones does **not** teach an aspect ratio greater than about one. At column 5, lines 3-9, Jones explicitly limits the aspect ratio possible through practicing his invention to no greater than 1: "Indeed lines as small as 2 mils wide and on 4 mils center can be employed in this invention." The examiner has not shown that Lan or any other prior art reference modifies Jones to teach the limitations claimed in claim 11. Therefore, for these reasons and for the reasons established in applicants' responsive amendment filed on November 29, 2001, claim 11 is believed to be allowable under 35 USC § 103(a) over the prior art of record.

Amended Claims 9, 10 and new claim 21. Claims 9 and 10 have been amended to incorporate limitations fully supported by the specification, and new claim 21 incorporates the same limitations. These limitations have been determined to be allowable in method claims 1-3 of related U.S. Patent No. 6,195,883 (serial number 09/047,984).

Specifically, amended claims 9, 10 and new claim 21 claim at least one filled plated through hole formed by depositing a seed layer on dielectric substrate and hole surfaces; depositing electrically conductive plating on the surfaces; filling said hole with a filler composition; partially etching said plating; removing residual amounts of filler composition; and etching to completely remove the plating. The resultant structure is distinct from and has advantages over the structures taught by Jones, Lan and the prior art of record, as supported and established in the specification at page 8, lines 3-13:

> An important facet of the invention herein is the process for preparing the subcomposite for full additive circuitization As a general overview of the process, conductive metal 14 must be removed down to dielectric substrate 10 prior to the additive plating of circuitry. The conductive metal is removed gradually, however, and a minimum thickness of conductive metal 14 remains until the process for removing the residual nubs of the cured fill compound 18 is nearly complete. *This is because the process for removing nubs of fill compound is harmful to substrate 10 and its receptivity to additive plating.*
> (Emphasis added.)

Furthermore, amended claims 9, 10 and new claim 21 claim circuitry on a dielectric substrate connected to the plated through hole, wherein the circuitry is formed by the steps of: depositing a seed activator on substrate, through hole and filler surfaces; covering said surfaces with a photoresist and exposing and developing the photoresist to reveal selected surface areas including the filler composition; and additively plating electrical circuitry on the selected areas *including circuitry on the filler composition* electrically connected to the plating on the hole surface (emphasis added). The resultant structure is additionally distinct from and has advantages over the structures taught by Jones, Lan and the prior art of record, as supported and established in the specification at page 10, line 29, through page 11, line 14:

> Additive plating also produces *pads 44* with the diameter of the *pads now capable of being approximately equal to the diameter of the landless, plated through holes.* In conventional methods, using for example the subtractive etch method of circuitization, the plating process is completed before the through holes are filled with compound. Thus, in conventional methods there is no layer of conductive metal plated over the filled through hole, which requires that a land of metal be made during the circuitization process to allow a solderable connection. *The additive plating method of the present*

invention eliminates the need for lands on the subcomposite around the plated through holes. Thus, as an added benefit of the invention herein, a larger surface area is available for both increased component density and increased wiring density. (Emphasis added.)

Therefore, for these reasons and for the reasons established in applicants' responsive amendment filed on November 29, 2001, amended claims 9, 10 and new claim 21 are believed to be allowable under 35 USC § 103(a) over the prior art of record.

Claims 12-20. Claims 12-20 are directly and indirectly dependent upon and include all of the limitations of amended claims 9 and 10 and claim 11 and are, therefore, for the above reasons and for the reasons established in applicants' responsive amendment filed on November 29, 2001, not properly rejected under 35 USC § 103 over the prior art of record.

Moreover, contrary to the examiner's assertion in his comments relevant to claims 12-14, Jones' land 14 structure does not teach the pad structure claimed by claims 12-14. Jones clearly teaches a conventional "land" 14. As established by his specification at column 2, lines 47-52, and in all of his figures, his land 14 is much larger than and disposed "around" the through holes 12. Nor has the examiner shown that the prior art of record modifies Jones to teach the pad claimed by claims 12-14.

In conclusion, the claims as amended and submitted are now believed to be in condition for allowance over the prior art of record. Applicants are providing clean and marked-up versions of the amended claims. As indicated earlier, one sheet of revised drawings is also being submitted.

Respectfully submitted,

Date: July 10, 2002

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Enclosures

END919960141US2 (IEN-10-5222-D1)